IN THE ABSTRACT:

The Abstract has been amended as follows:

A semiconductor memory device ~~is comprised~~ includes of a plurality of sense amplifiers. The sense amplifiers are arranged in two amplifier columns. The two amplifier columns are disposed between two cell columns of cell plates. An address circuitry, an ATD circuitry, and a delay circuitry are disposed between an input pin row and the two cell columns. An ATD pulse synthesizer is disposed between the two amplifier columns and spaced a predetermined signal transmission path from the ATD and delay circuitries.

AMENDMENTS TO THE DRAWINGS:

The attached annotated and replacement sheets of drawings includes changes to Fig. 4 which replaces the original sheet of Fig. 4. In Figure 4 previously omitted element 102 (shown in Figure 2) has been added.